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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,484	03/07/2002	Kazuo Goto	03500.016264	9461

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EXAMINER

POKRZYWA, JOSEPH R

ART UNIT PAPER NUMBER

2625

DATE MAILED: 06/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	10/091,484	GOTO, KAZUO	
	<b>Examiner</b>	<b>Art Unit</b>	
	Joseph R. Pokrzywa	2625	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 27 February 2006.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-15 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## DETAILED ACTION

### *Response to Amendment*

1. Applicant's amendment was received on 2/27/06, and has been entered and made of record. Currently, **claims 1-15** are pending.

### *Response to Arguments*

2. Applicant's arguments filed 2/27/06 have been fully considered but they are not persuasive.
3. Upon review of the reference of Nishizawa (U.S. Patent 5,661,373), which was cited in the Office action dated 9/20/05 as anticipating claims 1-10, the examiner notes that the reference still can be interpreted as anticipating the claims, as currently amended.
4. In response to applicant's arguments regarding the rejection of claim 1, whereby applicant argues on pages 8 and 9 that Nishizawa fails to teach of the feature of controlling a buffer to release a data signal line after the data signal line is temporarily retained at a second level, if a control signal for instructing a release of the data signal line is input when the data signal line is at a first level. Nishizawa states in column 11, lines 4-8, that "a High-level signal is outputted from the buffer amplifier BU1, and the output terminal of the buffer amplifier BU2 becomes a high impedance state". Continuing, in column 11, lines 31-35, that "the output terminal of the buffer amplifier BU1 becomes a high impedance state, and a Low-level signal is outputted from the buffer amplifier BU2 becomes the Low level". Thus, the buffer amplifier BU1 controls the buffer BU2 to release the data signal line (being the output of the buffer BU2).

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The signal line is released after the data signal line is temporarily retained at a second level (being temporarily in the low impedance state), if a control signal for instructing a release of the data signal line is input when the data signal line is at a first level (being the high impedance state). This is further exemplified in the timing chart of Fig. 8, whereby when the buffer BU2 is in the High level, control signals of the buffer amplifier release the output of the buffer BU2 so that the buffer BU2 releases to a Low level. Thus, Nishizawa teaches of buffer means (being the three-state buffer BU2) capable of releasing the data signal line (column 2, lines 14-51, and column 11, lines 1-57), and control means (being the buffer amplifier BU1) for controlling the buffer means to release the data signal line after the data signal line is temporarily retained at a second level, if a control signal for instructing a release of the data signal line is input when the data signal line is at a first level (see Fig. 8, column 2, lines 14-51, and column 10, line 51-column 11, line 57), as currently required in claim 1.

5. Therefore, currently amended claims 1 and 6, as well as newly added claim 11 are rejected with the previously cited reference in the Office action dated 9/20/05, wherein claims 1 and 6 were rejected under 35U.S.C.102(b) as being anticipated by Nishizawa, are maintained and repeated in this Office action.

***Claim Rejections - 35 USC § 102***

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. **Claims 1-15** are rejected under 35 U.S.C. 102(b) as being anticipated by Nishizawa (U.S. Patent Number 5,661,373, cited in the Office action dated 9/20/05).

Regarding **claim 1**, Nishizawa discloses a serial communication apparatus for sending and receiving serial data through data signal lines (see Fig. 2, column 2, lines 14-51, and column 10, lines 51-64), comprising buffer means (being the three-state buffer BU2) capable of releasing the data signal line (column 2, lines 14-51, and column 11, lines 1-57), and control means (being the buffer amplifier BU1) for controlling the buffer means to release the data signal line after the data signal line is temporarily retained at a second level, if a control signal for instructing a release of the data signal line is input when the data signal line is at a first level (see Fig. 8, column 2, lines 14-51, and column 10, line 51-column 11, line 57).

Regarding **claim 2**, Nishizawa discloses the apparatus discussed above in claim 1, and further teaches that the buffer means is a three-state buffer (column 10, lines 51-64, buffer BU2) for placing the data signal line in one of a high-output impedance level in the release state, the first level and the second level (column 11, lines 1-57, see Fig. 8).

Regarding **claim 3**, Nishizawa discloses the apparatus discussed above in claim 1, and further teaches of means for stopping an operation of the control means (column 10, lines 39-64, and column 11, lines 52-57).

Regarding **claim 4**, Nishizawa discloses the apparatus discussed above in claim 1, and further teaches of means for stopping an operation of the control means when a communication trouble occurs, and the operation of the control means (column 10, lines 39-64, and column 11, lines 52-57), is restarted when a normal communication is made after communication trouble occurs (column 10, lines 39-64, and column 11, lines 52-57).

Regarding **claim 5**, Nishizawa discloses the apparatus discussed above in claim 1, and further teaches that the control means controls the buffer means to release the data signal line if

the data signal line is at the first level when sending or receiving has ended (column 11, lines 1-57, see Fig. 8).

Regarding **claim 6**, Nishizawa discloses a serial communication method of sending and receiving serial data through a data signal line (see Fig. 2, column 2, lines 14-51, and column 10, lines 51-64), comprising a first step of temporarily retaining the data signal line at a second level, if a control signal for instructing a release of the data signal line is input when the data signal line is at a first level (see Fig. 8, column 2, lines 14-51, and column 10, line 51-column 11, line 57), and a second step of releasing the data signal line after retaining the data signal line at the second level in the first step (see Fig. 8, column 2, lines 14-51, and column 10, line 51-column 11, line 57).

Regarding **claim 7**, Nishizawa discloses the method discussed above in claim 6, and further teaches that the method uses a three-state buffer (column 10, lines 51-64, buffer BU2) for placing the data signal line in one of a high-output impedance level in the release state, the first level and the second level (column 11, lines 1-57, see Fig. 8).

Regarding **claim 8**, Nishizawa discloses the method discussed above in claim 6, and further teaches of a step of inhibiting the release of the data signal line (column 10, lines 39-64, and column 11, lines 52-57).

Regarding **claim 9**, Nishizawa discloses the method discussed above in claim 6, and further teaches of a step of inhibiting the release of the data signal line when a communication trouble occurs (column 10, lines 39-64, and column 11, lines 52-57), and a step of allowing the release of the data signal line when a normal communication is made after the communication trouble occurs (column 10, lines 39-64, and column 11, lines 52-57).

Regarding **claim 10**, Nishizawa discloses the method discussed above in claim 6, and further teaches of a step of releasing the data signal line if the data signal line is at the first level when sending or receiving has ended (column 11, lines 1-57, see Fig. 8).

Regarding **claim 11**, Nishizawa discloses a serial communication apparatus for sending and receiving serial data through a data signal line (see Fig. 2, column 2, lines 14-51, and column 10, lines 51-64), comprising a buffer (being the three-state buffer BU2) capable of releasing the data signal line (column 2, lines 14-51, and column 11, lines 1-57), and a controller (being the buffer amplifier BU1) which controls the buffer to release the data signal line after the data signal line is temporarily retained at a second level, if a control signal for instructing a release of the data signal line is input when the data signal line is at a first level (see Fig. 8, column 2, lines 14-51, and column 10, line 51-column 11, line 57).

Regarding **claim 12**, Nishizawa discloses the apparatus discussed above in claim 11, and further teaches that the buffer is a three-state buffer (column 10, lines 51-64, buffer BU2) which places the data signal line in one of a high-output impedance level in the release state, the first level and the second level (column 11, lines 1-57, see Fig. 8).

Regarding **claim 13**, Nishizawa discloses the apparatus discussed above in claim 11, and further teaches of a circuit which stops an operation of the controller (column 10, lines 39-64, and column 11, lines 52-57).

Regarding **claim 14**, Nishizawa discloses the apparatus discussed above in claim 11, and further teaches of a circuit which stops an operation of the controller when a communication trouble occurs, (column 10, lines 39-64, and column 11, lines 52-57), and restarts the operation

of the controller when a normal communication is made after communication trouble occurs (column 10, lines 39-64, and column 11, lines 52-57).

Regarding *claim 15*, Nishizawa discloses the apparatus discussed above in claim 11, and further teaches that the controller controls the buffer to release the data signal line, if the data signal line is at the first level when sending or receiving has ended (column 11, lines 1-57, see Fig. 8).

### ***Conclusion***

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

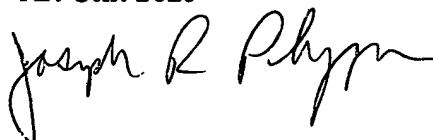
7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joe Pokrzywa whose telephone number is (571) 272-7410. The examiner can normally be reached on Monday-Friday, 9:00-5:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Edward L. Coles can be reached on (571) 272-7402. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Joseph R. Pokrzywa  
Primary Examiner  
Art Unit 2625



jrp